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Original scientific paper

# PROGRESS IN MATERIALS FOR MICROELECTRONICS AND FURTHER CHALLENGES

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Development of materials and technologies for microelectronics is required by the needs of the constantly increasing level of integration of microelectronics circuits. Increase of the integration level compels downscaling of all the dimensions of devices, which in its turn requires very thin layers with exceptional quality due to rather high electric fields at working conditions. First, technological improvements are adopted aimed at fabrication of materials with uniform quality, geometrical flatness and extremely low density of intentionally introduced defects. Second, new fabrication methods are developed providing materials with much better quality. Third, new materials showing better properties than the standard (conventional) ones are obtained and developed further.

Decreasing the dimensions of the layers changes the nature of the physical phenomena involved in the functioning of devices. Quantum mechanical mechanisms are more and more important in the description of the properties of the materials and devices on the nanoscale. The question arises where is the limit of the possibilities of the materials and technologies for nanoscale electronics.

Key words: microelectronics; ultrathin layers; limits of the scaling

# INTRODUCTION

Progress of microelectronics is a basis for development of all modern industries, as well as for the changes in the social communications. Constantly increasing level of integration of microelectronics integrated circuits (IC) requires materials used in the fabrication of these circuits to display extraordinary quality, precisely controlled properties and extremely low density of critical defects.

Devices that are fabricated are based on some basic structures that are illustrated in Figures 1 to 3. In Figure 1 a simple MOS structure is shown. MOS structure is a part of more complex structures, but it presents also a specific device – the MOS capacitor of a Dynamic Random Access Memory (DRAM). In Figure 2 the structure of a MOSFET is shown (metal-oxide-silicon field effect transistor). In Figure 3.a) a schematic representation of a memory device of type EEPROM is shown and in Figure 3.b) that of a charge trapping flash (CTF). In CTF memories the charges are located at spatially discrete traps distributed in the band gap of charge trapping layer, unlike the conventional floating gate memories where charges are stored in the conduction band of floating gate.



Figure 1. Schematic representation of a simple MOS structure



Figure 2. Schematic representation of a MOSFET device





(b) charge trapping flash

**Figure 3.** Schematic representaion of an EEPROM (a) and charge trapping flash (b)

# SUBSTRATE MATERIALS

Substrate bulk material is crucial for fabrication of devices and integrated microelectronics circuits. High quality semiconductrors with extremly low densities of defects are required as starting material in fabrication.

## Silicon

Standard material that has been used for many decades in mictroelectronics is monocristalline Silicon. Silicon crystallizes in diamond crystalline structure (cubic, Fd3m) with latice parameter 0.54311 nm at 300 K. It is a typical indirect semiconductor: thermal band gap is 1.12 eV and optical bandgap connected to direct transitions of electrons from the highest valence band maximum in the  $\Gamma$ point (center of the Brillouin zone) to the lowest conduction band minimum in the  $\Gamma$  point is 3.4 eV.Static relative permittivity of silicon is 11.9.

Nowadays fabrication technology allows obtaining monocrystalline silicon ingots twelve inches in diameter (30 cm). Ingots of next generation with diameter of 450 mm are envisioned. Silicon wafers for fabrication of integrated circuits are cut from large ingots.

#### Germanium

Germanium was a material used in the begining of the microelectronics era and then leaving its place to silicon, the later being identified as more appropriate for microelectronics applications. Thermal band gap of germanium is 0.66 eV and the optical band gap 0.8 eV.

Neverhtless, recently new perspectives for use of this material have been demonstrated [1],[2], due to the high mobility of carriers.

# SiC

Silicon carbide crystallizes in more than 200 different polytypes with cubic (zinc blende) unit cell, with hexagonal (wurtzite) unit cell and withrhombohedral unit cell. It is rather convenient for high temperature and/or high power devices[3].

## GaAs

Galium arsenide crystalizes in cubic zinc blende structure. It's a typical direct semiconductor having band gap of 1.424 eV at 300 K. Due to its high electron mobility (8500 cm<sup>2</sup>/(V·s)), it is used in ultrafast devices[4].

#### GaN

Gallium nitride is obtained in form of films deposited on foreign substrates (heteroepitaxy) [5].Standard techniques of crystal growth generally used for the growth of semiconductor substrates (such as Bridgman or Czochralski) cannot be used for GaN and only few techniques are available for single crystal growth [6].The use of GaAs in optoelectronic device is particularly important [7].

#### NEW MATERIALS

## Graphene

Graphene is a two-dimensional (2D) monolayer of sp2-bonded carbon atoms in a dense honeycomb crystal structure which behaves as a zerogap semiconductor with exceptionalelectronic quality [8]. In order to be used for microelectronics application, graphene has to be grown on convenient substrates bytechniques compatible with other processes used in fabrication of microelectronics devices. Large-area graphene on SiGe can be fabricated by atmospheric pressure CVD, which is convenient commercial deposition method; the fieldeffect transistors fabricated on such films are ofgood quality [9].Graphene can be also grown on Ge(001)/Si(001) [10].

#### $MoS_2$

Molybdenum disulphide ( $MoS_2$ ) is also one of the thinnest known materials with electronic properties that can be advantageous for a wide range of applications in nanotechnology. It can also be used in combination with graphene for fabrication of devices such as nonvolatile memory cells [11].

### Nanowire based devices

Starting material for fabrication of devices can also be one dimensional, such as nanowires [12]. Fabrication of devices starting from nanowires is demonstrated in many works [13].

### DIELECTRICS

A particularly important issue related to the further miniaturization of electron devices in nanoscale is that of the ultrathin dielectics. Dielectrics of outstanding quality are required for majority of the devices. Reliable function of the devices and hence the integrated circuits requires dielectrics that can be used at extremely high fields, of the order of 10 MV/cm without significant degradation.

## $SiO_2$

Silicon dioxide has an exceptional position among the dielectrics for use in silicon microelectronics. First, it grows starting from the silicon substrate in oxygene atmosphere. Second, it has very good interface with silicon and rather low density of bulk and interfacial defects. Various modifications of silicon dioxide have been studied in connection with applications in microelectronics, such as:  $\alpha$ -quartz,  $\beta$ -quartz,  $\beta$ tridymite,  $\alpha$ -crystobalite,  $\beta$ -crystobalite, keatite, coesite [14]. It appears that the best match between the single crystal silicon and silicon dioxide layer occurs for  $\beta$ -tridymite if the SiO<sub>2</sub> layer is very thin (~0.7 nm), when tridymite is energetically stable; as the SiO<sub>2</sub> layer becomes as thick as 1.5 nm, the quartz phase becomes stable [15], [16].

SiO<sub>2</sub> is the main reason that microelectronics uses Si technology and not another semiconductor. The use of SiO<sub>2</sub> as a gate dielectric offers several advantages. Amorphous SiO<sub>2</sub> can be thermally grown on Si with excellent control in thickness and uniformity, and naturally forms a stable, high quality Si–SiO<sub>2</sub> interface. SiO<sub>2</sub> has a very large band gap of 9.0 eV and large energy band offsets with the conduction (CB) and valence (VB) bands of Si, which ensure superior insulation properties and high breakdown field of about 13 MV/cm. SiO<sub>2</sub> shows an excellent thermal stability in contact with Si, which is required in order to withstand the thermal process steps up to 1000 °C.

#### Silicon oxynitride

It has been demonstrated that nitridation (typically in NH<sub>3</sub> and N<sub>2</sub>O) substantially improves dielectric and reliability properties of SiO<sub>2</sub> films on silicon. These layers are of variable composition and arereffered as silicon oxynitride (SiO<sub>x</sub>N<sub>y</sub>, Si–O–N). There are optimal conditions for nitridation [17], [18] leading to incorporation of about 6 % of a monoatomic layer of N atoms at the interface between the silicon and the oxide layer [19].

Silicon dioxide and silicon oxynitrideultra thin film far below 4 nm in thickness approach their electrical limits for applications in microelectronic devices [20], [21], mainly due to direct tunnelling of electrons through the dielectric (SiO<sub>2</sub> thinner than 2 nm).

#### High permittivity dielectrics

As a solution to this problem, high permittivity dielectrics (high- $\kappa$ ) are used as a replacement for silicon dioxide in various applications [22], [23], [24].

Materials used as high- $\kappa$  dielectrics are: Al<sub>2</sub>O<sub>3</sub> [25], Ta<sub>2</sub>O<sub>5</sub>, SrTiO<sub>3</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub> [26], HfO<sub>2</sub> [27], La<sub>2</sub>O<sub>3</sub>, Lu<sub>2</sub>O<sub>3</sub>, Sc<sub>2</sub>O<sub>3</sub>, Dy<sub>2</sub>O<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, etc. For illustration, values of relative permittivity ( $\varepsilon_{hk}$ ) and band gap ( $E_g$ ) of some high- $\kappa$  dielectrics are shown in Table 1. For comparison, relative permittivity and band gap for silicon dioxide are  $\varepsilon(SiO_2) = 3.9$ and  $E_g(SiO_2) = 8.97$  eV. The main advantage of high- $\kappa$  dielectrics compared to SiO<sub>2</sub> comes from their substantially higher values of relative permittivity (about one order of magnitude). Thus, the same capacitance of a capacitor containg high- $\kappa$  dielectric could be obtained with substantially larger physical thicknesses compared to  $SiO_2$ , which leads to substantially lower leakage currents due to tunnelling.

**Table 1.** Relative permittivity ( $\varepsilon_{hk}$ ) and band gap ( $E_g$ ) of some high- $\kappa$  dielectrics

high-κ	$Al_2O_3$	Ta <sub>2</sub> O <sub>5</sub>	$La_2O_3$	HfO <sub>2</sub>	TiO <sub>2</sub>	ZrO <sub>2</sub>
$E_{\rm g}({\rm eV})$	8.8	4.4	4.5	5.7	3.5	7.8
$\mathcal{E}_{\mathrm{hk}}$	9	26	30	25	80	25

However, the above benefit is reduced by the lower values of band offsets related to the band gap. Roughly, as a measure of the benefit of using high- $\kappa$  dielectric instead of SiO<sub>2</sub>, the ratio *r* defined with equation (1) can be used [28]:

$$r = \frac{\varepsilon_{\rm hk} / \varepsilon(\rm{SiO}_2)}{E_{\rm g} / E_{\rm g}(\rm{SiO}_2)}.$$
 (1)

More detailed comparison of high- $\kappa$  dielectrics is given in [29] where figure of a merit that connects two main properties of the gate stack, namely, the leakage current and the capacitance is used.

A particular phenomenon occuring in metal/high- $\kappa$ /silicon structures is the reaction with the silicon substrate and in some cases (reactive gate) with the metal gate. Thus, instead of the MOS structure depicted in Figure 1, structures shown in Figure 4 are obtained [30]. Interfacial layer between the Si substrate and high- $\kappa$  can be silicon oxide or silicate.

In our works we extensively studied tantalum pentoxide high-k layers on silicon. Interfacial layer for films of good quality is SiO<sub>2</sub>-like layer [31]. In the case of nonreactive gate, the obtained MOS structure is metal/Ta2O5/SiO2/Si. Electrical and reliability properties of such a structure can be precisely described by a comprehensive model we described in [32]. Using this model, we explained the increased leakage in the case of reactive Al gates compared to the case of nonreactive Ag and W as caused by the creation of defects in Ta<sub>2</sub>O<sub>5</sub> due to reaction with Al [33]. Stress induced leakage currents have been explained by creation of conductive paths in the SiO<sub>2</sub> interfacial layer leading to a decrease of its effective dielectric thickness [34]. Review of the results obtained using the model mentioned above are given in [35]. Band diagram used in the model is shown in Figure 5.

High- $\kappa$  dielectrics are also used with Ge as a substrate [36].



(a) a simple MOS structure containg high- $\kappa$  dielectric and additional interfacial layer with Si substrate



(b) or both interfacial layer with Si substrate and interfacial layer with metal gate



Optimum properties can be obtained by using nanolaminated, dopped and mixed oxides such as lanthanum gadolinium oxide [37], HfGdO/HfTiO [38], Al-doped TiO<sub>2</sub> [39], Gd doped HfO<sub>2</sub> [40], HfO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> [41], HfTiO/Y<sub>2</sub>O<sub>3</sub> [42], SrTa<sub>2</sub>O<sub>6</sub> [43], Gd<sub>2</sub>O<sub>3</sub>/HfSiO [44] etc.

MOS structures containing high- $\kappa$  exhibit some particularities that are not present in metal/SiO<sub>2</sub>/semiconductor structures. Most important, frequency dispersion of the capacitance is observed that is not due to real variations of the relative permittivity of the material with the frequency of the measurement signal [45], [46], [47]. An effect of charge trapping at the contact between high work function and metal gate high- $\kappa$  has been observed

[48], [49]. Charging of the intereface between high- $\kappa$  and the interfacial layer also occurs, leading to modification of *C-V* characteristics [50].



Figure 5. Detailed band diagram of a metal/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si structure.  $\phi_e$  and  $\phi_h$  are band offsets for electrons and holes relative to the Si substrate and  $\phi'_e$  and  $\phi'_h$  are band offsets for electrons and holes relative to the high- $\kappa$  dielectric.

Flash memories for future generations are also based on the use of high permittivity dielectrics [51], [52]. With using nanocrystals as floating gate, higher data retention and faster program/erase speeds are obtained [53].

A particular effect used in memory devices is the resistive switching [54], [55]. Resistive switching is a kind of reversible change of electronic conductivity in thin films under electrical stress. Some high- $\kappa$ materials with suitable properties are used in memory devices based on resistive switching.

### Gate materials

In the beginning of the microelectronic era, the main material for gates was aluminium. Later, it was replaced by aluminium, since Al creates significant damage to the silicon dioxide thin dielectric layers.

The use of high permittivity dielectrics raised the interest for various metal gates [56].We have recently demonstrated that Ag gates provide particularly good electrical properties of MOS structures containing high- $\kappa$  dielectric [57].

# MATERIALS FOR SPECIFIC APPLICATIONS

#### Green electronics

Research in materials for microelectronics leading to biodegradable and biocompatible devices becomes more and more important; it is uslually known as "green" electronics [58]. As substrate paper is used (semi-natural/semi-synthetic substrate), synthetic polymers (biocompatible substrate) natural silk, shellac, hard gelatin (fully biocompatible and biodegradable substrates), as well as other materials. Fully resorbable and biodegradable dielectrics are also used.

#### Perovskite manganites

Nanosized perovskite manganites exhibit novel properties usefull for application in microelectronics, such as colossal magneto-resistance, magnetocaloric effect, multiferroic property, and some interesting physical phenomena including spin, charge, and orbital ordering [59].

#### Multiferroic materials

Multiferroic materials represent a novel class of material where multiple types of ferroic ordering coexist, and their coupling can lead to additional ordering parameters [60].

## FUTURE TRENDS

Materials for microelectronics with exceptionally high quality have been developed in last decades.

Altough various substrate materials with extraordinary properties have been developed, crystal silicon remains the main material for new generation of microelectronic circuits.

Particular position between the materials belongs to dielectrics. High permittivity dielectrics have been developed as a replacement of silicon dioxide for various applications.

#### REFERENCES

- P. S. Goley, M. K. Hudait, Germanium Based Field-Effect Transistors: Challenges and Opportunities, *Materials*, 7 (2014), pp. 2301–2339.
- [2] N. M. Bom, G. V. Soares, S. Hartmann, A. Bordin, C. Radtke, GeO<sub>2</sub>/Ge structure submitted to annealing in deuterium: Incorporation pathways and associated oxide modifications, *Appl. Phys. Lett.*, **105** (2014), 141605-1–141605-4.
- [3] F. La Via, M. Camarda, A. La Magna, Mechanisms of growth and defect properties of epitaxial SiC, *Appl. Phys. Rev.*, 1 (2014), pp. 031301-1–031301-36.
- [4] L. Hu, J. Su, Z. Ding, Q. Hao, X, Yuan, Investigation on properties of ultrafast switching in a bulk gallium arsenide avalanche semiconductor switch, *J. Appl. Phys.*, **115** (2014), 094503-1–094503-10.
- [5] L. Liu, J. H. Edgar, Substrates for gallium nitride epitaxy, *Mater. Sci. Eng. R.*, **37** (2002), pp. 61–127.
- [6] A.Denis, G. Goglio, G. Demazeau, Gallium nitride bulk crystal growth processes: A review, *Mater. Sci. Eng. R*, **50** (2006), pp. 167–194.
- [7] J. Wu, S. Chen, Al. Seeds, H. Liu, Quantum dot optoelectronic devices: lasers, photodetectors and solar cells, *J. Phys. D: Appl. Phys.*, 48(2015), pp. 363001-1–363001-28.
- [8] K. Geim, K.S. Novoselov, The rise of graphene, *Nature Materials*, **6** (2007), pp.183–191.
- [9] D. Chen, G. Wang, J. Li, Q. Guo, LinYe, H. Zhou, L. Zheng, M. Zhang, S. Liu, Graphene film synthesis on SiGe semiconductor substrate for field-effect transistor, *Materials Letters*, **135** (2014), pp. 222– 225.

- [10] G. Lippert, J. Dąbrowski, T. Schroeder, M. A. Schubert, Y. Yamamoto, F. Herzige, J. Maultzsch, J. Baringhaus, C. Tegenkamp, M. C. Asensio, J. Avila, G. Lupina, Graphene grown on Ge(001) from atomic source, *Carbon*, **75** (2014), pp. 104–112.
- [11] S. Bertolazzi, D. Krasnozhon, A. Kis, Nonvolatile Memory Cells Based on MoS<sub>2</sub>/Graphene Heterostructures, ACS Nano, 7 (2013), pp. 3246–3252.
- [12] W. M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, T. Mikolajick, Reconfigurable nanowire electronics – A review, *Solid-St. Electron.*, **102** (2014), pp. 12–24.
- [13] M. Fu, D. Pan, Y. Yang, T. Shi, Z. Zhang, J. Zhao, H. Q. Xu, Q. Chen, Electrical characteristics of field-effect transistors based on indium arsenide nanowire thinner than 10 nm, *Appl. Phys. Lett.*, **105** (2014), pp. 143101-1–143101-3.
- [14] С. С. Некрашевич, В. А. Гриценко, Электронная структура оксида кремния (Обзор), Физика твердого тела, 56 (2014), pp. 209–223; S. S. Nekrashevich, V. A. Gritsenko, Electronic structure of silicon dioxide (a review), Physics of the Solid State, 56 (2014), pp. 207–222.
- [15] T. Yamasaki, C. Kaneta, T. Uchiyama, T. Uda, K. Terakura, *Phys. Rev. B*, **63** (2001), pp. 115314-1– 115314-5.
- [16] K. Xue, H. P. Ho, J. B. Xu, Local study of thickness-dependent electronic properties of ultrathin silicon oxide near SiO<sub>2</sub>/Si interface, *J. Phys. D: Appl. Phys.*,**40** (2007), pp. 2886–2893.
- [17] N. Novkovski, M. Dutoit, J. Solo de Zaldivar, Dielectric breakdown in thin Si oxynitride films produced by rapid thermal processing, *Appl. Phys. Lett.*,56(1990), pp.2120–2122.
- [18] M. Dutoit, P. Letourneau, J. Mi, N. Novkovski, J. Manthey, J. Solo de Zaldivar, Optimization of thin Si oxynitride films produced by rapid thermal processing for applications in EEPROMs, *J. Electrochem. Soc.*, **140** (1993), pp. 549–555.
- [19] N. Novkovski, On the impeded growth of oxide films on Si in N<sub>2</sub>O ambient, *Appl. Phys. A*, 68 (1999), pp. 573-575.
- [20] M. L. Green, E. P. Gusev, R. Degraeve, E. L. Garfunkel, Ultrathin (< 4 nm) SiO<sub>2</sub> and Si–O–N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits, *J. Appl. Phys.*, **90** (2001), pp. 2057–2121.
- [21] N. Novkovski, E. Atanassova, Approaching the limit of the SiO<sub>2</sub> possibilities for application in nanoscale microelectronics, J. Optoelectron.Adv. Mat., 8 (2006), pp. 1238–1242.
- [22] J. Robertson, High dielectric constant gate oxides for metal oxide Si transistors, *Rep. Prog. Phys.*, 69 (2006), pp. 327–396.

- [23] J. H. Choi, Y. Mao, J. P. Chang, Development of hafnium based high-k materials-A review, *Mater. Sci. Eng. R*, 72 (2011), pp. 97–136.
- [24] S. K. Ray, R. Mahapatra, S. Maikap, High-k gate oxide for silicon heterostructure MOSFET devices, *J. Mater. Sci.: Mater. Electron.*,17 (2006), pp. 689–710.
- [25] X. Qin, H. D., J. Kim, R. M. Wallace, A crystalline oxide passivation for Al<sub>2</sub>O<sub>3</sub>/AlGaN/GaN, *Appl. Phys. Lett.*,**105** (2014), pp. 141604-1–141604-5.
- [26] D. Panda, T.-Y. Tseng, Growth, dielectric properties, and memory device applications of ZrO<sub>2</sub> thin films, *Thin Solid Films*, **531** (2013), pp. 1–20.
- [27] M. Barth, G. B. Rayner Jr., S. McDonnell, R. M. Wallace, B. R. Bennett, R. Engel-Herbert, and S. Datta, High quality HfO<sub>2</sub>/p-GaSb(001) metaloxide-semiconductor capacitors with 0.8 nm equivalent oxide thickness, *Appl. Phys. Lett.*, **105** (2014), pp. 222103-1–222103-5.
- [28] N. Novkovski, Peculiarities of the interface between high-permittivity dielectrics and semi–conductors, *Front. Mater.*, 1 (2014), pp. 30-1–30-3.
- [29] J.-P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine, J. W. Seo, J. Appl. Phys., 100 (2006), pp. 051610-1–051610-14.
- [30] H. Wong, J. Zhang, S. Dong, K. Kakushima, H. Iwai, Thermal annealing, interface reaction, and lanthanum-based sub-nanometer EOT gate dielectrics, *Vacuum*, **118** (2015), pp. 2–7.
- [31] E. Atanassova, M. Kalitzova, G. Zollo, A. Paskaleva, A. Peeva, M. Georgieva, G. Vitali, High temperatureinduced crystallization in tantalum pentoxide layers and its influence on the electrical properties, *Thin Solid Films*, **426** (2003), pp. 191–199.
- [32] N. Novkovski, E. Atanassova, A comprehensive model for the I-V characteristics of metal Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>-Si structures, *Appl. Phys. A*, 83 (2006), pp. 435–445.
- [33] N. Novkovski, E. Atanassova, Injection of holes from the silicon substrate in Ta<sub>2</sub>O<sub>5</sub> films grown on silicon, *Appl. Phys. Lett.*, **85** (2004), pp. 3142–3144.
- [34] N. Novkovski, E. Atanassova, Origin of the stressinduced leakage currents in Al-Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>-Si structures, *Appl. Phys. Lett.*, **86** (2005), pp. 152104-1–152104-3.
- [35] N. Novkovski, Physical modeling of electrical and dielectric properties of high-κ Ta<sub>2</sub>O<sub>5</sub> based MOS capacitors on silicon, *FactaUniversitatis: Electronics and Energetics*, **27** (2014), pp. 259–273.
- [36] Y. Kamata, High-*k*/Ge MOSFETs forfuture nanoelectronics, *Materials Today*, **11** (2008), pp. 30–38.
- [37] Sh. P. Pavunny, J. F. Scott, R. S. Katiyar, Lanthanum Gadolinium Oxide: A New Electronic Device Material for CMOS Logic and Memory Devices, *Materials*, 7 (2014), pp. 2669–2696.

- [38] J. W. Zhang, G. He, H. S. Chen, J. G. Lv, J. Gao, R. Ma, M. Liu, Z. Q. Sun, Comparison of mictrostructure and electrical characteristics of sputteringderived HfGdO/HfTiO and HfTiO/HfGdO gate stacks, *Ceramics International*, **41** (2015), pp. 10216–10221.
- [39] L. Aarik, T. Arroval, R. Rammula, H. Mändar, V. Sammelselg, B. Hudec, K. Hušeková, K. Fröhlich, J. Aarik, Atomic layer deposition of high-quality Al<sub>2</sub>O<sub>3</sub> and Al-doped TiO<sub>2</sub> thin films from hydrogen-free precursors, *Thin Solid Films*, **565** (2014), pp. 19–24.
- [40] X. Zhang, H. Tu, Y. Guo, H. Zhao, M. Yang, F. Wei, Y. Xiong, Z. Yang, J. Du, W. Wang, Atomic configuration of the interface between epitaxial Gd doped HfO<sub>2</sub> high k thin films and Ge(001) substrates, *J. Appl. Phys.*, **111** (2012), pp. 014102-1-014102-4.
- [41] E. Atanassova, A. Paskaleva, D. Spassov, Doped Ta<sub>2</sub>O<sub>5</sub> and mixed HfO<sub>2</sub>-Ta<sub>2</sub>O<sub>5</sub> films for dynamic memories applicationsat the nanoscale, *Microelectron. Reliab.*, **52** (2012), pp. 642–650.
- [42] B.-Y. Tsui, H.-H. Hsu, C.-H. Cheng, Highperformance metal-insulator-metal capacitors with HfTiO/Y<sub>2</sub>O<sub>3</sub> stacked dielectric, *IEEE Electron. Dev. Lett.*, **31** (2010), pp. 871–877.
- [43] P. F. Zhang, R. E. Nagle, N. Deepak, I. M. Povey, Y. Y. Gomeniuk, E. O'Connor, N. Petkov, M. Schmidt, T. P. O'Regan, K. Cherkaoui, M. E. Pemble, P. K. Hurley, R. W. Whatmore, The structural and electrical properties of the SrTa<sub>2</sub>O<sub>6</sub>/In<sub>0.53</sub>Ga<sub>0.47</sub>As/InP system, *Microelectron. Eng.*, **88** (2011), pp. 1054–1057.
- [44] J. A. Caraveo-Frescas, M. N. Hedhili, H. Wang, U. Schwingenschlögl, H. N. Alshareef, Anomalous positive flatband voltage shifts in metal gate stacks containing rare-earth oxide capping layers, *Appl. Phys. Lett.*, **100** (2012), pp. 102111-1–102111-4.
- [45] J. Tao, C. Z. Zhao, C. Zhao, P. Taechakumput, M. Werner, S. Taylor, P. R. Chalker, Extrinsic and Intrinsic Frequency Dispersion of High-κ Materials in Capacitance-Voltage Measurements, *Materials*, 5 (2012), pp. 1005-1032.
- [46] N. Novkovski, E. Atanassova, Frequency dependence of the effective series capacitance of metal-Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>-Si structures, *Semicond. Sci. Technol.*, **22** (2007), pp. 533–536.
- [47] N. Novkovski, E. Atanassova, Peculiarities of capacitance measurements of nanosized high-κ dielectrics: case of Ta<sub>2</sub>O<sub>5</sub>, J. Optoelectron. Adv. Mat.-Symposia, 1 (2009), pp. 398–403.
- [48] N. Novkovski, A. Skeparovski, E. Atanassova, Charge trapping effect at the contact between a high-work-function metal and Ta<sub>2</sub>O<sub>5</sub> high-κdielectric, J. Phys. D: Appl. Phys., **41** (2008), pp. 105302-1–105302-4.

- [49] L. Stojanovska-Georgievska, N. Novkovski, E. Atanassova, Charge trapping at Pt/high-κ dielectric (Ta<sub>2</sub>O<sub>5</sub>) interface, *Physica B: Condensed Matter*, **406** (2011), pp. 3348–3353.
- [50] N. Novkovski, Determination of interface states in metal (Ag, TiN, W)-Hf : Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>x</sub>N<sub>y</sub>-Si structures by different compact methods, *Materi. Sci. Semicond. Proc.*, **39** (2015), pp. 308–317.
- [51] C. Zhao, C. Zh. Zhao, St. Taylor, P. R. Chalker, Review on Non-Volatile Memory with High-k Dielectrics:Flash for Generation Beyond 32 nm, *Materials*,7 (2014), pp. 5117–5145.
- [52] J.-C. Wang, C.-T. Lin, P.-C. Chou, C.-S. Lai, Gadolinium-based metal oxide for nonvolatile memory applications, *Microelectron. Reliab.*, 52 (2012), pp. 635–641.
- [53] S. K. Ray, S. Maikap, W. Banerjee, S. Das, Nanocrystals for silicon-basedlight-emitting and memory devices, J. Phys. D: Appl. Phys., 46 (2013), 153001-1–153001-31.
- [54] D. B. Strukov, H. Kohlstedt, Resistive switching phenomena in thin films: Materials, devices, and applications, *MRS Bull.*, **377** (2012), pp. 108–114.

- [55] M. Lanza, A Review on Resistive Switching in High-k Dielectrics: A Nanoscale Point of View Using Conductive Atomic Force Microscope, *Materials*, 7 (2014), pp. 2155–2182.
- [56] J. Robertson, R. M. Wallace, High-K materials and metal gates for CMOS applications, *Mater. Sci. Eng. R.*, 88 (2015), pp. 1–41.
- [57] N. Novkovski, E. Atanassova, Leakage current characteristics of metal (Ag, TiN, W)-Hf : Ta<sub>2</sub>O<sub>5</sub>/Si-O<sub>x</sub>N<sub>y</sub>–Si structures, *Mater. Sci.Semicond. Proc.*,29 (2015), pp. 345–350.
- [58] M. Irimia-Vladu, "Green" electronics: biodegradable and biocompatible materials and devices for sustainable future, *Chem. Soc. Rev.*, **43** (2014), pp. 588–610.
- [59] T. Zhang, X. P. Wang, Q. F. Fang, X. G. Li, Magnetic and charge ordering in nanosized manganites, *Appl. Phys. Rev.*, **1** (2014), pp. 031302-1–031302-21.
- [60] J. S. Andrew, J. D. Starr, M. A. K. Budi, Prospects for nanostructured multiferroic composite materials, *Scripta Materialia*, **74** (2014), pp. 38–43.

### НАПРЕДОК ВО МАТЕРИЈАЛИТЕ ЗА МИКРОЕЛЕКТРОНИКАТА И ИДНИ ПРЕДИЗВИЦИ

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Потребата од постојано зголемување на степенот на интеграција на микроелектронските кола изискува развиток на материјали и технологии за микроелектрониката. Порастот на степенот на интеграција бара намалување на сите димензии на уредите, што од своја страна изискува добивање на мошне тенки слоеви со исклучителен квалитет поради особено силните електрични полиња при работните услови. Прво, се усвојуваат технолошки подобрувања со цел изработка на материјали со рамномерен квалитет, геометриска мазност и крајно ниска густина на ненамерно внесени дефекти. Второ, се развиваат нови методи за изработка на материјали со многу подобар квалитет. Трето, се добиваат и понатаму се развиваат нови материјали што покажуваат подобри својства од стандардните.

Намалувањето на димензиите на слоевите ја менува природата на физичките појави вклучени во функционирањето на уредите. Квантномеханичките ефекти стануваат сè позначајни за опишувањето на својствата на материјалите и уредите од наноскалата. Се поставува прашањето каде се границите на можностите на материјалите и технологиите за електрониката на наноскалата.

Клучни зборови: микроелектроника; ултратенки слоеви; граници на скалирањето